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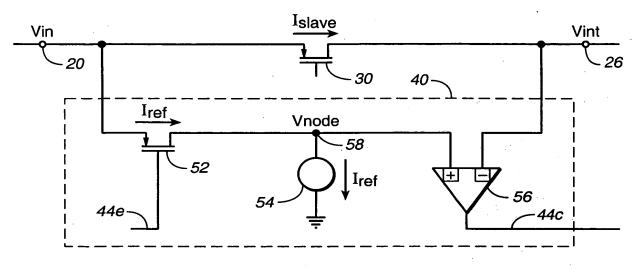
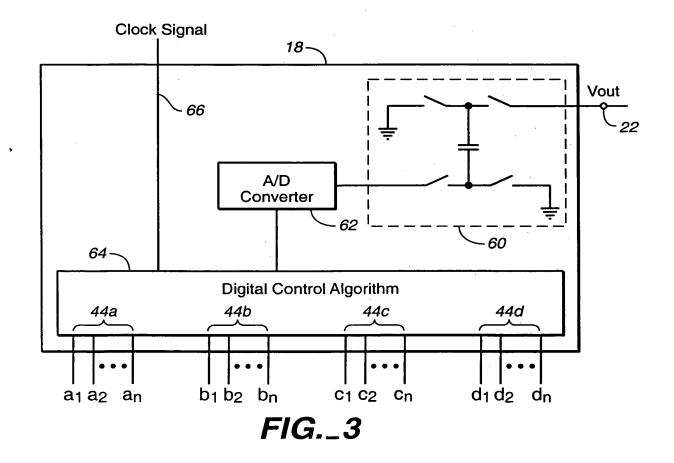
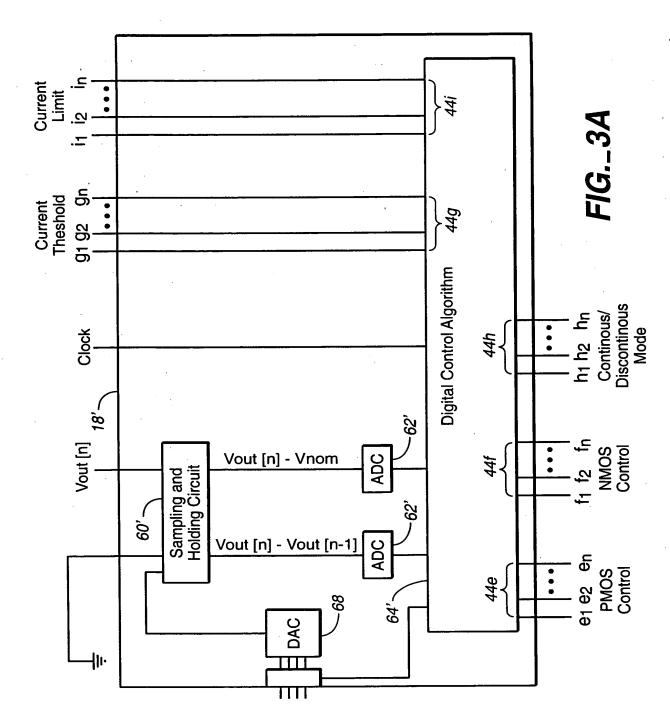


FIG._2





1



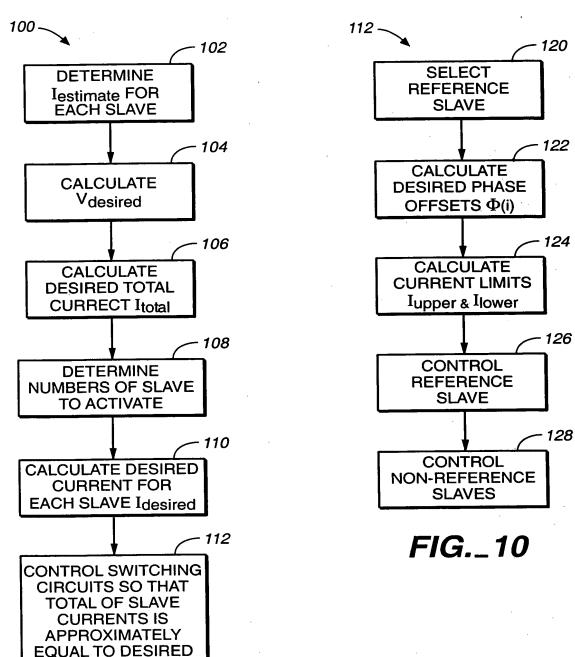


FIG._4

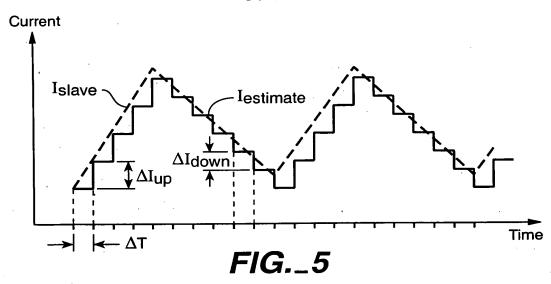
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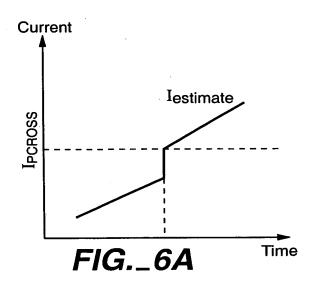
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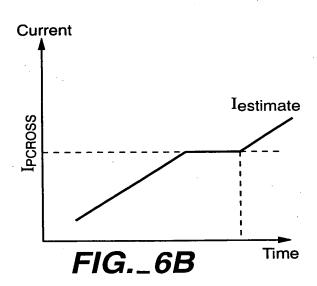
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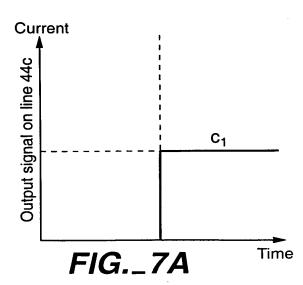


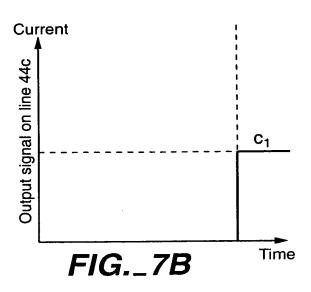












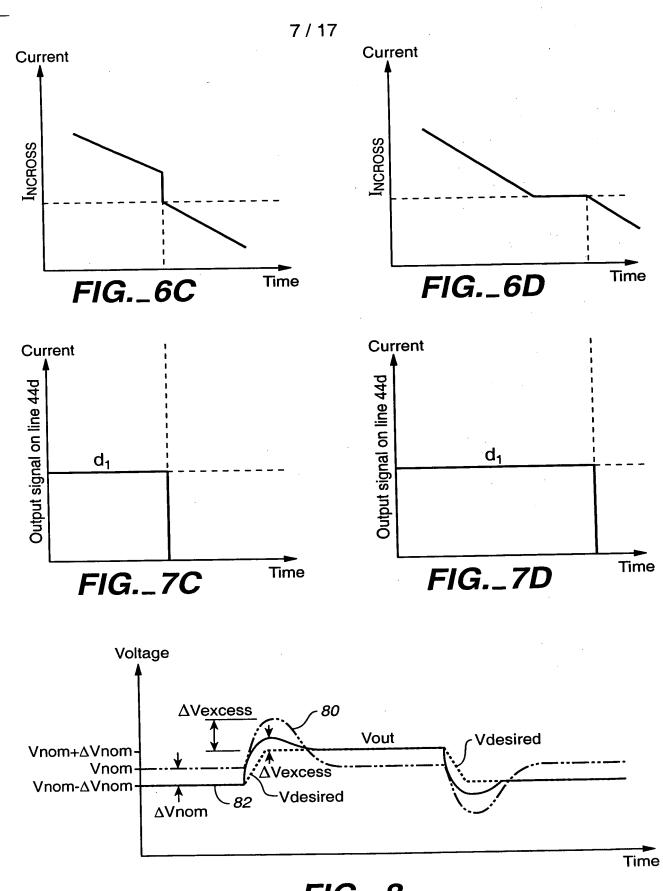
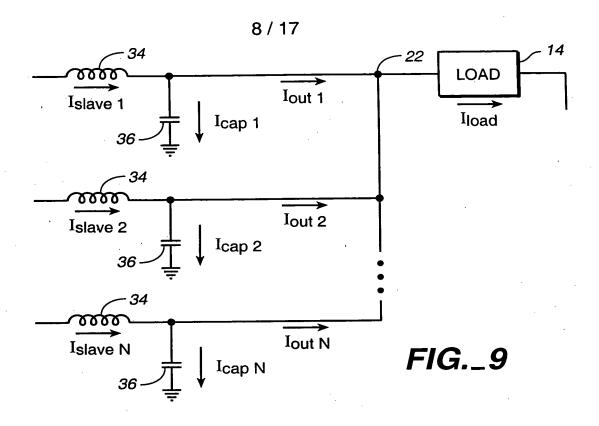


FIG._8



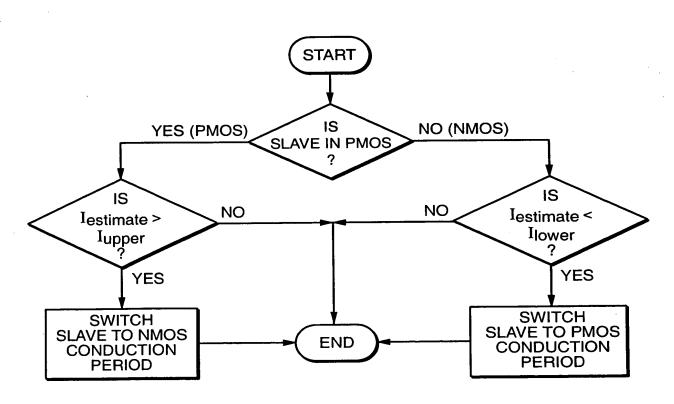
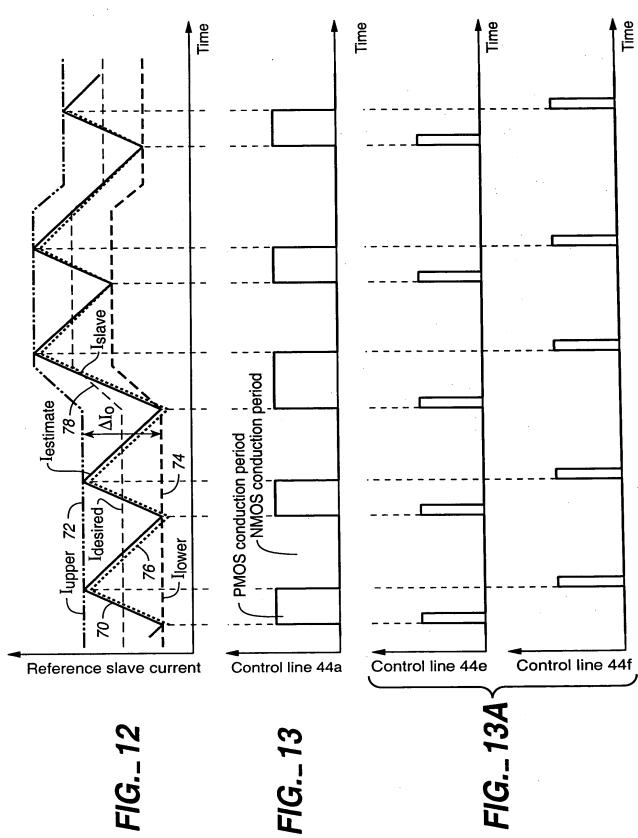
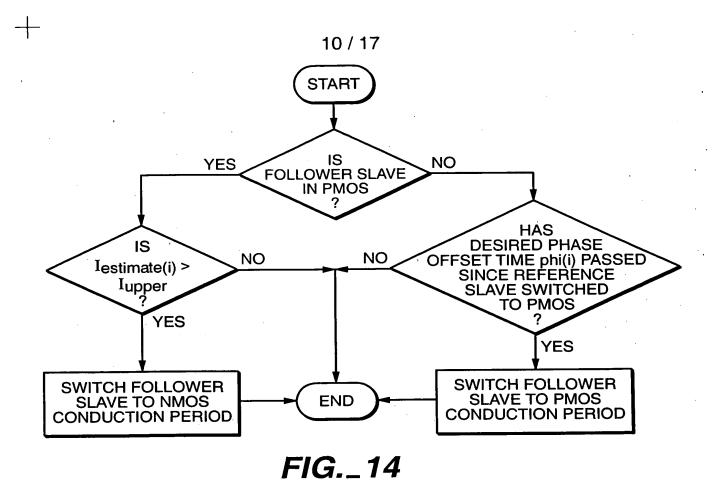


FIG._11





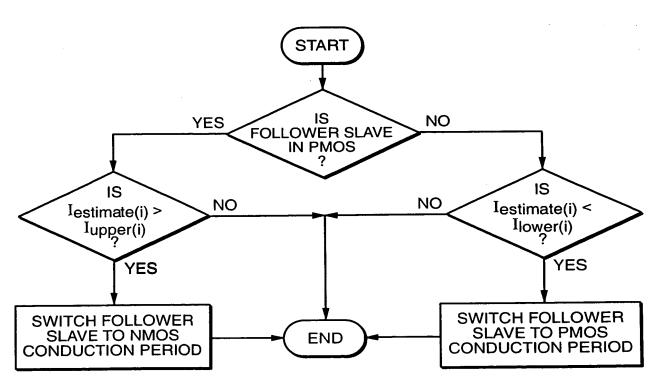
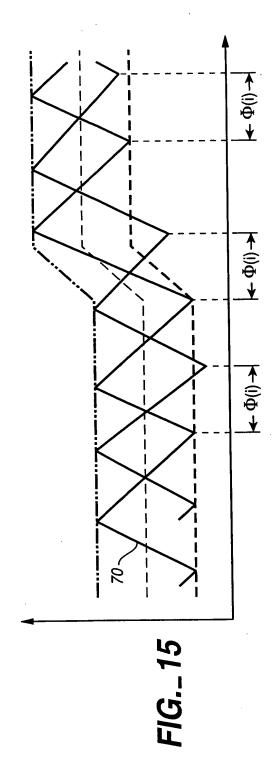
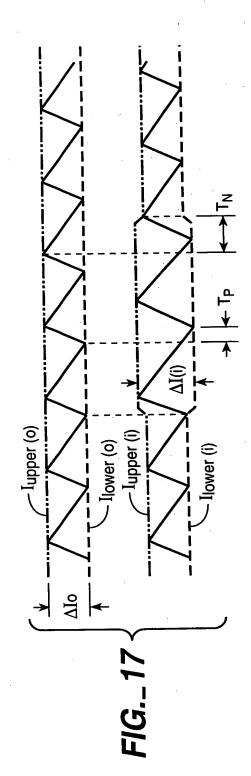
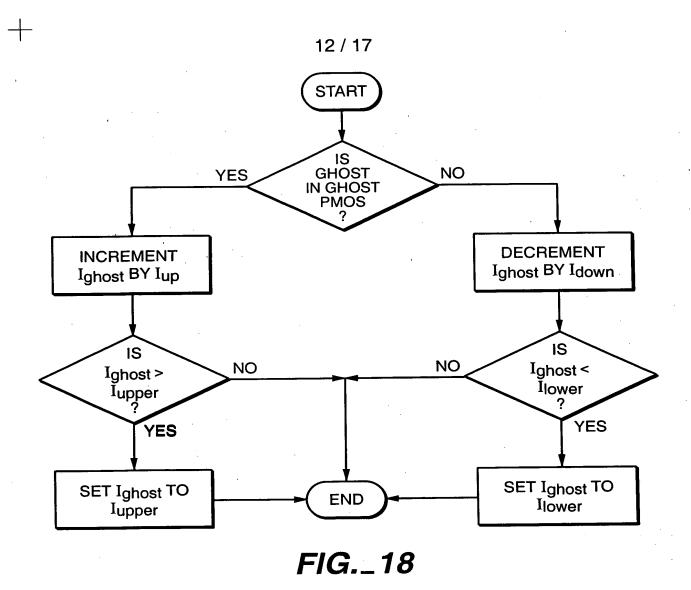


FIG._16





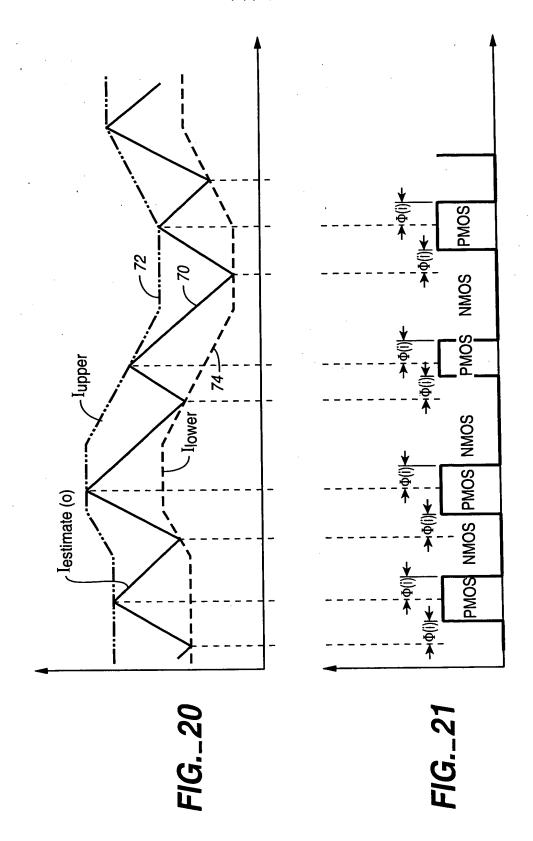
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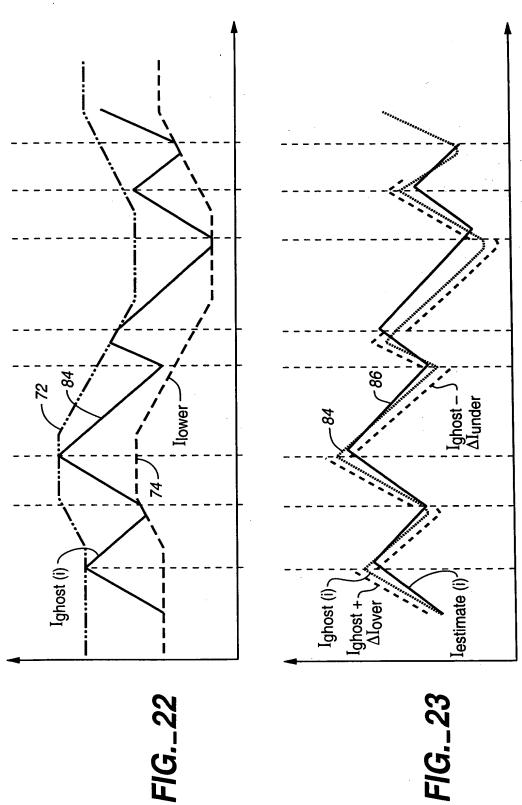
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13 / 17 START FOLLOWER NO YES SLAVE IN PMOS IS GHOST IN PMOS GHOST IN NMOS YES YES NO NO IS lestimate < IS NO NO Iestimate > Ighost Ighost **YES** YES IS Iestimate(i) < YES YES Îestimate(i) > Ighost(i) - Iunder Ighost(i) + Ìover NO NO **SWITCH SWITCH** FOLLOWER SLAVE TO **FOLLOWER SLAVE TO PMOS** NMOS CONDUCTION CONDUCTION PERIOD **PERIOD END**

FIG._19



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16/17 **START** SLAVE IN PMOS YES NO GHOST IN NMOS IS GHOST IN PMOS YES YES NO NO IS Iestimate < Ighost IS NO NO Iestimate > Ighost **YES** YES IS IS Is Iestimate(i) < YES YES Iestimate(i) > Ilower ? NO NO SWITCH SLAVE TO PMOS CONDUCTION **SWITCH** SLAVE TO NMOS CONDUCTION PERIOD **PERIOD END**

FIG._24

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